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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/594,844

09/28/2006

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Q97404

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23373 7590 05/07/2009
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EXAMINER

HARRISTON, WILLIAM A

ART UNIT

PAPER NUMBER

2826

MAIL DATE

DELIVERY MODE

05/07/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/594,844	Applicant(s) OHUCHI ET AL.	
	Examiner WILLIAM HARRISTON	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 11 February 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4,6,8,9 and 11-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4,6,8,9 and 11-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>9/28/2006</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-4, 5-9, 11 and 12 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4, 6, 8, 9 and 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Qi US 6774497 taken with Fujimori US 20040046252 A1.
4. Regarding claim 1, figures 1-4 of Qi et al. disclose a semiconductor device (200) comprising:

a wiring board (240) in which electrode pads (242) are formed on the surface thereof;

a semiconductor element (210) which is disposed on the wiring board and in which electrodes (214) are formed on the surface thereof;

bumps (220) for connecting said electrodes (214) to said electrode pads (242);

said bumps (220) being formed from solder; and

an underfill material (230) filled between said wiring board (240) and said semiconductor element (210) to embed said bumps, wherein said wiring board comprises a solder resist (250) disposed on the surface of the side on which said

electrode pads (242) are formed;

wherein apertures for exposing said electrode pads (242) are formed on the solder resist (Examiner has interpreted "apertures" to be openings formed in the solder resist layer, this feature is disclosed at column 6, line 49-51) and the thickness of said solder resist in the area excluding the area directly above said electrode pads is equal to or greater than the thickness of said underfill resin disposed on said solder resist in said area between said wiring board and said semiconductor element. See column 7.

Figure 4 of Qi discloses wherein the volume of said bumps (220) is greater than the volume of said apertures.

Qi et al. does not disclose the underfill material is resin. However, figure 43 of Fujimori et al. does disclose a resin underfill material (173). It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Qi with the teachings of Fujimori because forming an under fill material from resin would reduce heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

5. Regarding claim 2, Qi et al. taken with Fujimori et al. disclose the device of claim 1 for the reasons stated above. Qi et al. further disclose the device wherein the thickness of said underfill resin disposed on said solder resist is 50 micrometers or less. See Qi et al. column 7, lines 1-6.

6. Regarding claim 4, Qi et al. taken with Fujimori et al. disclose the device of claim 3 for the reasons stated above. Qi et al. further disclose the device wherein the thickness of said solder resist (250) is 30 micrometers or more. See Qi et al. column 6 lines 60-62.

7. Regarding claim 6, figures 1-3 of Qi et al. disclose a method for manufacturing a semiconductor device comprising the steps of forming bumps (120) on at least one element selected from said electrode pads(114) and said electrodes (242) (310), depositing an underfill material (130) on at least a portion of the area in which said semiconductor element (110) is to be mounted on said wiring board (240) (320), pressing said semiconductor element to said wiring board to connect said electrode pads, said bumps, and said electrodes to each other, melting and then solidifying said bumps to join said electrodes to said electrode pads by way of said bumps, and curing said resin material and forming an underfill resin so that said bumps become embedded between said wiring board and said semiconductor element, wherein the distance between said wiring board and said semiconductor element is controlled during the melting of said bumps in said joining step, and the thickness of said solder resist in the area excluding the area directly above said electrode pads is equal to or greater than the thickness of said underfill material disposed on said solder resist in said area between said wiring board and said semiconductor element after said underfill material has been formed. See columns 7 and 8.

Figure 2b of Qi discloses wherein the volume of said bumps 120 /220 is less than the volume of said apertures in the step of forming said bumps.

Qi et al. does not disclose the underfill material is resin. However, figure 43 of Fujimori et al. does disclose a resin underfill material (173). It would have been obvious to one having skill in the art at the time the invention was made to combine the teachings of Qi with the teachings of Fujimori because forming an under fill material from resin would reduce heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

8. Regarding claim 8, Qi et al. taken with Fujimori et al. disclose the method of claim 7 for the reasons stated above. Qi et al. further disclose the method wherein the thickness of said solder resist (250) is 30 micrometers or more. See column 6.

9. Regarding claim 9, Qi et al. taken with Fujimori et al. disclose the method of claim 8 for the reasons stated above. Qi et al. further disclose the method wherein the distance between said wiring board and semiconductor element is controlled by controlling the relative position of said semiconductor element with respect to said wiring board in said joining step. See column 7.

10. Regarding claim 11, Qi et al. taken with Fujimori et al. disclose the method of claim 6 for the reasons stated above. Qi et al. further disclose an underfill material to which a chemical capable of removing an oxide film is added is used as an underfill material. See column 7, line 52- column 8.

Qi et al. does not disclose the underfill material is resin. However, figure 43 of Fujimori et al. does disclose a resin underfill material (173). It would have been obvious

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to one having skill in the art at the time the invention was made to combine the teachings of Qi with the teachings of Fujimori because forming an under fill material from resin would reduce heat induced deformation between a semiconductor element and a wiring board which improves the reliability of connections. Further, since the gap between the semiconductor element and the wiring board is sealed by resin, corrosion can be prevented by keeping moisture away from the solder balls and electrodes.

11. Regarding claim 12, Qi et al. taken with Fujimori et al. disclose the device of claim 6 for the reasons stated above. Qi taken with Fujimori do not disclose the step of carrying out a plasma treatment. However, plasma treatment is well known in the art for growing largely crystalline oxide coating, which present high hardness and a continuous barrier, on metals. One of ordinary skill in the art would be motivated to perform a plasma treatment for the purpose of offering protection against wear, corrosion, and heat.

12. Regarding claims 13 and 15, Qi taken with Fujimori disclose the device of claim 1 and the method of claim 6 for the reasons stated above. Qi further discloses wherein the thickness of the solder resist (250) is about 30 micrometers. See Qi column 7, lines 1-21.

13. Regarding claims 14 and 16, Qi taken with Fujimori disclose the device of claim 1 and the method of claim 6 for the reasons stated above. Qi further discloses wherein:

the thickness of the solder resist 250 in the area excluding the area directly above the electrode pads is at least four times greater than the thickness of the underfill

resin 230 disposed on the solder resist in the area between the wiring board 240 and the semiconductor element 210. See Qi column 7 lines 1-6.

Conclusion

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILLIAM HARRISTON whose telephone number is (571)270-3897. The examiner can normally be reached on Monday - Friday 9 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on (571)272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. H./

Examiner, Art Unit 2826

/VICTOR A MANDALA JR/

Examiner, Art Unit 2826

5/4/09